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@INPROCEEDINGS{1595640,
author={Netto, E.W. and Billo, E. and Azevedo, R.},
journal={ International Symposium on System-on-Chip, 2005},
title={Exploiting the Area X Performance Trade-off with Code
Compression \.
year={2005},
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volume={},
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abstract={Code compression has been shown to be efficient in code
size reduction and, recently in performance improvement. In this
paper we use a compression method, the ComPacket, which has a very
fast decompressor in hardware, to compress selective regions of the
code (the inner-loops) to improve performance and in the
complementary regions we use the instruction based compression (IBC)
method to sustain the code size reduction both at the same time.
Using the Leon (SPARC v8) platform and benchmarks from Mediabench
and MiBench suites we reached 29% of memory area reduction, on
average, and a speed-up of 1.8 simultaneously.},
keywords={ComPacket;Leon platform;Mediabench;MiBench suites;RISC
processors; SPARC v8; code compression; code size reduction; instruction
based compression; memory area reduction; cache storage; instruction
sets; microprocessor chips; reduced instruction set computing; },
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