

The advent of new 90 nm/130 nm VLSI technology and SoC design methodologies, has brought an explosive growth in the complexity of modern electronic circuits. As a result, functional verification has become the major bottleneck in any design flow. New methods are required that allow for easier, quicker and more reusable verification. In this paper we propose an automatic verification methodology approach that enables fast, transaction-level, coverage-driven, self-checking and random-constraint functional verification. Our approach uses the systemC verification library (SCV), to synthesize a tool capable of automatically generating testbench templates. A case study from a real MP3 design is used to show the effectiveness of our approach.