

In this report we introduce a new architecture description language (ADL) called ArchC. ArchC is an open-source SystemC-based ADL that is specialized for processor architecture description. Its main goal is to provide enough information, at the right level of abstraction, in order to allow users to explore and verify new architectures, by automatically generating simulators, assemblers and compiler back-ends. ArchC's key feature is a storage-based co-verification mechanism that automatically checks the consistency of refined SystemC RTL models against the behavioral reference model. We have used ArchC to synthesize cycle-based simulators for the MIPS, Intel 8051 and SPARC processors.