

@ARTICLE{959861,
author={Rajagopalan, S. and Rajan, S.P. and Malik, S. and Rigo, S.
and Araujo, G. and Takayama, K.},
journal={IEEE Transactions on Computer-Aided Design of Integrated
Circuits and Systems},
title={A retargetable VLIW compiler framework for DSPs with
instruction-level parallelism},
year={2001},
month=nov,
volume={20},
number={11},
pages={1319 -1328},
keywords={DSP chips;Fujitsu Hiperion fixed-point DSP;SoC
design;assembly code generation;digital signal processor;embedded
processors;enhanced IMPACT framework;execution time
improvement;highly retargetable optimizing compilers;instruction-
level parallelism;irregular architectures;retargetable VLIW compiler
framework;system-on-a-chip design;very long instruction word
processor;digital signal processing chips;embedded
systems;instruction sets;optimising compilers;parallel
architectures;},
doi={10.1109/43.959861},
ISSN={0278-0070},}