The design of new architectures can be simplified with the use of retargetable instruction set simulation tools, which can validate the design decisions in the design exploration cycle with high flexibility and reduced cost. The growing system complexity makes the traditional approach inefficient for today's architectures. Compiled simulation techniques make use of a priori knowledge to accelerate the simulation, with the highest efficiency achieved by employing static scheduling techniques. This paper presents our approach to the static scheduling compiled simulation technique that is 90% faster than the best published performance results. It also introduces two novel optimization techniques based on instruction type information that further increase the simulation speed by more than 100%. The so-called fast static compiled simulation (FSCS) technique applicability will be demonstrated by the use of the SPARC and MIPS architectures.