

The increasing complexity of modern System-on-Chip (SoC) platforms has revealed the need for methodologies that enable a rigorous engineering design process, based on a combination of Electronic System Level (ESL) description languages, and IP-core modeling and reuse. On the other hand, ESL modeling has faced designers with the same methodology problems encountered in the design of large computer programs. In this paper, we describe a SystemC-only IP-core design process, called IP PROCESS (IPP). IPP is inspired on two rigorous software engineering processes (RUP and XP), and on well-known hardware design standards (VSIA and RMM). The IPP Verification Methodology (IPV) is based on a careful refinement of the SystemC behavioral description towards RTL. Such approach enabled a continuous co-simulation against the behavioral reference model, while allowed for a SystemC-only environment. As a result, we have experienced a considerable reduction in design time and an improvement in early bug detection. The IPP process has been used by over 70 designers of the BrazilIP Network, a SystemC collaborative partnership, in the design of the Fenix system. An intermediate step in the Fenix design is a real-world multimedia platform called CINE-IP (demo available at <http://www.brazilip.org.br/cine-ip>), composed of MPEG4, MP3 decoders and an 8051 microcontroller. The application of the IPP methodology in the design of CINE-IP, and its impact in design productivity is thoroughly analyzed.