This paper[3.5pc] presents the Platform Designer (PD) framework, a set of SystemC based tools that provide support for modeling, simulation and analysis of multiprocessor SoC platforms (MPSoC), at different abstraction levels. PD provides mechanisms for interconnection specification, process synchronization and communication, thus allowing the modeling of a complete platform, in a unified environment. To do that it uses an extension of the ArchC ADL and acsys, a tool that enables the automatic generation of a SystemC simulator of the platform. The main advantages of this approach are twofold. First, designers have more flexibility since they can integrate and configure different processors to the platform, using a single environment. Second, it enables a faster design space exploration, given that it automatically generates SystemC simulators of whole platforms at distinct abstraction levels. A number of platform variations can be tried out with minor design changes, thus reducing design time. Experimental results show the suitability of the platform simulator for design space exploration. Real applications (with medium complexity) run in the platform in few minutes. Combined with the facility to generate platforms with minor changes, this feature allows an improvement of the design space exploration.