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@INPROCEEDINGS{520610,  
author={Araujo, G. and Malik, S.},  
booktitle={Proceedings of the Eighth International Symposium on  
System Synthesis},  
title={Optimal code generation for embedded memory non-homogeneous  
register architectures},  
year={1995},  
month=sep,  
volume={},  
number={},  
pages={36 -41},  
keywords={ TMS320C25 processor; embedded memory nonhomogeneous  
register architectures; expression trees; instruction selection;  
instruction set architecture; optimal code generation; register  
allocation; register transfer graph; scheduling; structural  
representation; sufficient conditions;[1, infin;] model;  
computational complexity; computer architecture; graph theory;  
instruction sets; microprocessor chips; optimisation; processor  
scheduling; storage allocation;},  
doi={10.1109/ISSS.1995.520610},  
ISSN={},}
```