Identity-Based Cryptography has been gradually accepted as a more effective way of implementing asymmetric cryptography.
The calculation of cryptographically-suitable pairings is crucial for the performance of pairing based protocols.
In this paper we present a comparative study of hardware implementation techniques for computing the ?T pairing over the finite field F_3^97.
Our hardware-software implementation use Altera Nios II processor as platform.
Using code profiling we identify critical field operations which concentrate most of the execution time;
then these operations were implemented as specialized FPGA instructions/modules and added to the processor.
The specialized processor was synthesized and the application was tailored to the new hardware.
Experimental results show that a considerable speedup can be achieved when compared to the baseline software only approach.
Moreover, we show that such HW/SW co-design approach is competitive with other solutions.